CERTIFICATE OF VERIFICATION

I, Su Hyun LEE of 648-23 Yeoksam-dong, Kangnam-ku, Seoul, Korea state that the attached document is a true and complete translation to the best of my knowledge of the Korean-English language and that the writings contained in the following pages are correct English translations of the specifications and claims of the Korean Patent Application No. P2002-44692.

Dated this 10th day of December 2004

Signature of translator: _____

Su Hyun LEE

[ABSTRACT]

An LCD device and a method for fabricating the same is disclosed, to form patterned spacers for maintaining a cell gap on an outside of an active region too for improving a cell gap yield, in which the LCD device includes first and second substrates having a dummy region and an active region; a main sealant on a periphery of the active region between the first and second substrates; a dummy sealant in the dummy region between the first and second substrates; a patterned spacer in the dummy region between the first and second substrates; and a liquid crystal layer in the active region between the first and second substrates.

[TYPICAL DRAWINGS]

FIG. 5

[INDEX]

patterned spacer, dummy sealant, EPD hole, liquid crystal display device

[SPECIFICATION]

[TITLE OF THE INVENTION]

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 illustrates a plan view of a sealant pattern in a related art LCD device.

FIG. 2A illustrates a layout of a thin film transistor array substrate according to the related art.

FIG. 2B illustrates a cross sectional view along I-I' of FIG. 2A.

FIG. 3A illustrates a layout of a color filter array substrate according to the related art.

FIG. 3B illustrates a cross sectional view along II-II' of FIG. 3A.

FIG. 4A illustrates a plane view of a related art LCD device having a defective cell gap by a dummy sealant.

FIG. 4B illustrates a cross sectional view along III-III' of FIG. 4A.

FIG. 5 illustrates a plane view of a sealant and a spacer in an LCD device according to the present invention.

FIG. 6A illustrates a layout of a first substrate of each panel area of FIG. 5.

FIG. 6B illustrates a cross sectional view along IV-IV' of FIG. 6A.

FIG. 7A illustrates a layout of a second substrate of each panel area of FIG. 5.

FIG. 7B illustrates a cross sectional view along V-V' of FIG. 7A.

FIG. 8 illustrates a cross sectional view along VI-VI' of FIG. 5.

FIG. 9A to FIG. 9D illustrate cross sectional views of the fabrication process for

a thin film transistor array substrate according to the present invention.

FIG. 10A to FIG. 10C illustrate cross sectional views of the fabrication process for a color filter array substrate according to the present invention.

Description of reference numerals for main parts in the drawings

1: first substrate	2a: gate electrode
3: data line	3a: source electrode
3b: drain electrode	4: pixel electrode
5: gate insulating film	6: semiconductor layer
7: protection film	8, 15: alignment film
9: contact hole	9a: EPD hole
10: main sealant	11: second substrate
12: black matrix layer	13: color filter layer
14: common electrode	16a, 16b: patterned spacer
17: liquid crystal layer	20: dummy sealant

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]

The present invention relates to a liquid crystal display (LCD) device and a method for fabricating the same, and more particularly, to an LCD device and a method for fabricating the same, in which patterned spacers for maintaining a cell gap are formed on an outside of an active region too for improving a cell gap yield.

Keeping pace with development of an information oriented society, demands on

displays increase gradually in a variety of forms, and, recently to meet the demands, different flat display panels, such as LCD (Liquid Crystal Display), PDP (Plasma Display Panel), ELD (Electro Luminescent Display), VFD (Vacuum Fluorescent Display), and the like, have been under development, and some of which are employed as displays in various apparatuses already.

The LCDs have been used the most widely as portable displays while the LCDs replaces the CRT (Cathode Ray Tube) owing to features and advantages of excellent picture quality, light weight, thin, and low power consumption. Besides the portable type LCDs, such as a monitor of a notebook computer, the LCDs are under development for TVs for receiving and displaying broadcasting signals, and monitors of computers.

Despite of the various technical developments on the LCDs for serving as displays in different fields, the studies for enhancing a picture quality of the LCDs as displays are inconsistent to the features and advantages of the LCD in many aspects. Therefore, for employing the LCD in various fields as general displays, a key of development of the LCDs lies on whether the LCDs can implement a high quality picture, such as a high definition, a high luminance, and a large sized screen while the LCDs are light weighted, and thin, and of low power consumption.

The LCD is provided with a liquid crystal display panel for displaying a picture, and a driving part for providing a driving signal to the liquid crystal display panel, wherein the liquid crystal display panel has first and second glass substrates bonded with a gap between the substrates, and a liquid crystal layer injected between the first and second glass substrates.

On the first glass substrate (a TFT array substrate), there are a plurality of gate lines arranged in one direction at fixed intervals, a plurality of data lines arranged in a

direction perpendicular to the gate lines at fixed intervals, a plurality of pixel electrodes in respective pixel regions defined at crossing portions of the gate lines and the data lines to form a matrix, and a plurality of thin film transistors switchable in response to a signal from the gate lines for transmission of a signal from the data line to the pixel electrodes.

On the second glass substrate (a color filter substrate), there are a black matrix layer for shielding a light from portions excluding the pixel regions, a color filter array having an R/G/B color filter layer for displaying colors, and a common electrode for implementing a picture. At this time, the common electrode may be formed on the first glass substrate in case of an IPS mode LCD device.

The foregoing first and second substrates are spaced by spacers, and bonded with sealant having a liquid crystal injection hole, through which liquid crystal is injected.

The liquid crystal is injected by evacuating the space between the bonded two substrates and dipping the liquid crystal injection hole in liquid crystal, when the liquid crystal flows in the space between the two substrates by the capillary tube phenomenon. Once the liquid crystal is injected, the liquid crystal injection hole is sealed by the sealant.

Since the fabrication of LCD by liquid crystal injection, in which thus the two substrates are bonded and the liquid crystal is injected between the two substrates, requires much fabrication time period and has a limitation in fabrication of a large sized LCD, recently a method is suggested, in which the liquid crystal is dropped on the substrate before the two substrates are bonded.

Accordingly, though the fabrication of LCD by liquid crystal injection requires

spreading of ball spacers before bonding the substrates for maintaining the cell gap between the two substrates, the fabrication of LCD by liquid crystal dispensing requires patterned spacer or column spacer fixed to the substrate because the ball spacer can not maintain the cell gap in the fabrication of LCD by liquid crystal dispensing.

Device and method for fabricating an LCD by using the patterned spacer will be described as follows. FIG. 1 illustrates a plan view of a sealant pattern in a related art LCD device.

In general, the LCD is not fabricated one by one individually, but, there may be difference in sizes, a plurality of LCDs (unit panels) are designed and fabricated on a large sized mother substrate, and subjected to scribing and breaking process, to separate individual LCDs.

FIG. 1 illustrates two mother substrates provided with a plurality of unit panels (active regions, A/A) arranged thereon, main sealant 10 for bonding the two substrate and maintaining the liquid crystal within an inside thereof, and dummy sealant 20 for uniform maintenance of a cell gap of the two bonded substrates in dummy regions other than the unit panels (active regions).

A first substrate having a thin film transistor array of each unit panel will be described as follows.

FIG. 2A illustrates a layout of a thin film transistor array substrate according to the related art. FIG. 2B illustrates a cross sectional view along I-I' of FIG. 2A.

As shown in FIG. 2A, on the first substrate for the thin film transistor array, there are a plurality of gate lines 2 arranged along a first direction at fixed intervals, a plurality of data lines 3 arranged along a second direction being in perpendicular to the first direction at fixed intervals, a plurality of pixel electrodes 4 formed in a matrix-type

configuration with respective pixel regions defined by crossing the gate and data lines 2 and 3 to each other, and a plurality of thin film transistors TFT being switched by signals of the gate lines 2 to transmit signals of the data lines 3 to the respective pixel electrodes 4.

As shown in FIG. 2A and FIG. 2B, the thin film transistors TFT includes a gate electrode 2a projecting from the gate line 2, a gate insulating film 5 formed on an entire surface of the first substrate 1 including the gate electrode 2a, an island-shaped semiconductor layer 6 formed on the gate insulating film above the gate electrode 2a, a source electrode 3a projecting from the data line 3 at one side of the semiconductor layer 6, and a drain electrode 3b formed in opposite to the source electrode 3a. Then, a protection film 7 is formed on the entire surface of the first substrate to have a contact hole 9 corresponding to the drain electrode 3b, and the pixel electrode 4 is formed in the pixel region for being connected with the drain electrode 3b by the contact hole 9. Also, an alignment film 8 is formed on the entire surface of the first substrate to align liquid crystal molecules.

Herein, as described above, each panel area (active region) has the thin film transistor array. However, an EPD hole (End Point Direction) 9a is formed in the dummy region to measure and control etching extent when forming the contact hole 9 by forming the protection film 7 and selectively etching the protection film 7 above the drain electrode 3b (in case of a pad region, the contact hole is formed by etching the gate insulating film 5 and the protection film 7).

That is, the contact hole 9 is formed for being narrow and deep above the drain electrode 3b. Thus, if excessively etching the protection film 7, the drain electrode 3b may be damaged. Or, if insufficiently etching the protection film 7, it may cause a

defective contact between the drain electrode and the pixel electrode. Accordingly, the EPD hole 9a is formed in the dummy region to control the etching extent of the contact hole 9.

A second substrate of a color filter array will be described as follows.

FIG. 3A illustrates a layout of a color filter array substrate according to the related art. FIG. 3B illustrates a cross sectional view along II-II' of FIG. 3A.

That is, the second substrate of the color filter array includes a black matrix layer 12 for preventing light leakage on remaining portions except the pixel regions, an R/G/B color filter layer 13 for displaying colors in the pixel regions, and a common electrode 14 formed on an entire surface of the second substrate including the R/G/B color filter layer 13. Also, patterned spacers 16 are formed at fixed intervals on the common electrode 14, and an alignment film 15 is formed on the entire surface of the second substrate including the patterned spacers 16 to align liquid crystal molecules. At this time, the patterned spacers 16 are formed on the active region in each panel area, and are not formed on the dummy region.

As shown in FIG. 1, the main sealant 10 is formed on the edge of the panel area, and the dummy sealant 20 is formed on the dummy region, and then liquid crystal is dropped onto the substrate, and the two substrates are bonded to each other.

However, the related art device and method for fabricating a liquid crystal display device have the following problems.

FIG. 4A illustrates a plane view of a related art LCD.device having a defective cell gap by a dummy sealant. FIG. 4B illustrates a cross sectional view along III-III' of FIG. 4A.

As described above, on formation of the EPD holes 9a and the dummy sealant

20 in the dummy region, in case the dummy sealant 20 is formed in the EPD hole 9a, a defective cell gap is formed due to the dummy sealant 20.

That is, the cell gap of a reflective or transmitting-reflective LCD is in a range of approx. 2.5μm. Though a depth of the EPD hole 9a varies on kind of the protection film, since the protection film is formed of an organic insulating material at a thickness of 2μm and the EPD hole 9a removes the gate insulating film too, the EPD hole 9a has a depth close to the cell gap. Therefore, if the dummy sealant 20 is formed in the EPD hole 9a, a defective cell gap is occurred due to the dummy sealant in bonding the two substrates, to form a gap spot 30 in the active region close to the EPD hole 9a.

For solving the foregoing problem, though it is required to move parts the dummy sealant are formed thereon, or to change formation positions of the EPD holes, the position changes of the EPD hole or the dummy sealant are difficult because it is difficult to provide a larger dummy region for increasing a utilization efficiency of the mother substrate. Moreover, the requirement of applying the same design rule for separating into unit panels makes the position change of the dummy sealant and the EPD hole difficult.

[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]

Accordingly, the present invention is directed to an LCD device and a method for fabricating the same that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an LCD device and a method for fabricating the same, in which patterned spacers for maintaining a cell gap are formed on an outside of an active region too for improving a cell gap yield.

[PREFERRED EMBODIMENTS OF THE INVENTION]

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a liquid crystal display device includes first and second substrates having a dummy region and an active region; a main sealant on a periphery of the active region between the first and second substrates; a dummy sealant in the dummy region between the first and second substrates; a patterned spacer in the dummy region between the first and second substrates; and a liquid crystal layer in the active region between the first and second substrates.

In another aspect, a method for fabricating a liquid crystal display device includes steps of providing first and second substrates having a dummy region and an active region; forming patterned spacers in the dummy region and the active region of one of the first and second substrates; forming a main sealant on a periphery of the active region and a dummy sealant in the dummy region of one of the first and second substrates; dispensing liquid crystal on the active region of one of the first and second substrates; and bonding the first and second substrates.

Hereinafter, an LCD device and a method for fabricating the same according to the present invention will be described with reference to the accompanying drawings.

FIG. 5 illustrates a plane view of a sealant and a spacer in an LCD device according to the present invention.

In state a plurality of unit panels (active regions, A/A) are arranged on the substrates, there are a main sealant 10 for bonding the two substrates and holding the liquid crystal therein, and a dummy sealant 20 in a dummy region to surround the main

sealant except the unit panels (active regions) for maintaining a cell gap between the bonded two substrates and protecting the main sealant 10. In addition, patterned spacers 16a and 16b are formed, not only in the active regions, but also in the dummy region.

A first substrate of a thin film transistor array of each unit panel according to the present invention will be described as follows.

FIG. 6A illustrates a layout of a first substrate of each panel area of FIG. 5. FIG. 6B illustrates a cross sectional view along IV-IV' of FIG. 6A.

As described above, as shown in FIG. 6A, the first substrate 1 of the thin film transistor array includes a plurality of gate lines 2 arranged in one direction at fixed intervals, a plurality of data lines 3 arranged in a direction perpendicular to the gate lines 2 at fixed intervals, a plurality of pixel electrodes 4 in respective pixel regions defined at cross points of the gate lines 2 and the data lines 3 to form a matrix, and a plurality of thin film transistors TFT switchable in response to a signal from the gate lines 2 for transmission of a signal from the data line 3 to the pixel electrodes 4.

As shown in FIG. 6A and FIG. 6B, the thin film transistor TFT includes a gate electrode 2a projecting from the gate line 2 on the first substrate 1, a gate insulating film 5 on an entire surface of the first substrate including the gate electrode 2a, an island-shaped semiconductor layer 6 on the gate insulating film 5 above the gate electrode 2a, a source electrode 3a projecting from the data line 3 at one side of the semiconductor layer 6, and a drain electrode at an opposite side of the source electrode 3a. Then, a protection film 7 is formed on the entire surface of the first substrate to have a contact hole 9 above the drain electrode 3b, and the pixel electrode 4 is formed in the pixel region for being connected with the drain electrode 3b by the contact hole 9.

In addition, an alignment film 8 is formed on the entire surface of the first substrate to align liquid crystal molecules.

At this time, as described above, each panel area (active region) has the thin film transistor array. However, an EPD hole (End Point Direction) 9a is formed in the dummy region to measure and control etching extent when forming the contact hole 9 by forming the protection film 7 and selectively etching the protection film 7 above the drain electrode 3b (in case of a pad region, the contact hole is formed by etching the gate insulating film 5 and the protection film 7).

That is, the contact hole 9 is formed for being narrow and deep above the drain electrode 3b. Thus, if excessively etching the protection film 7, the drain electrode 3b may be damaged. Or, if insufficiently etching the protection film 7, it may cause a defective contact between the drain electrode and the pixel electrode. Accordingly, the EPD hole 9a is formed in the dummy region to control the etching extent of the contact hole 9.

A second substrate of a color filter array will be described as follows.

FIG. 7A illustrates a layout of a second substrate of each panel area of FIG. 5. FIG. 7B illustrates a cross sectional view along V-V' of FIG. 7A.

On the second substrate 11, there are black matrix layers 12 for shielding a light from parts except the pixel region, R, G, B color filter layers 13 in respective pixel region for displaying colors, and a common electrode 14 on an entire surface of the second substrate inclusive of the color filter layer 13 for implementing a picture. There are patterned spacers 16a and 16b on the common electrode 14 at fixed intervals, and an alignment film 15 on the entire surface of the substrate including the patterned spacers 16a and 16b for orienting the liquid crystal. In this instance, the

patterned spacers 16a and 16b are formed, not only in the active regions of the panels, but also the dummy regions of the panels, wherein the patterned spacer 16a in the active region is for maintaining the cell gap of the substrates, and the patterned spacer 16b in the dummy region is for prevention of occurrence of defective cell gap at the dummy sealant 20 due to the EPD hole 9a. Although not shown in the drawing, there may be the black matrix layer 12 formed in the vicinity of the patterned spacer 16a for prevention of occurrence of light leakage caused by defective orientation in the vicinity of the patterned spacer 16a when the alignment film 15 is rubbed.

Like that, as shown in FIG. 5, the main sealant 10 is formed in a periphery of respective panel regions, the dummy sealant 20 is formed to surround the main sealant 10 on the first substrate or the second substrate, the liquid crystal is dropped on the first or second substrates, and then the two substrates are bonded.

FIG. 8 illustrates a cross sectional view along VI-VI' of FIG. 5.

As described above, even if the EPD hole 9a is formed in the dummy region and the dummy sealant 20 is formed in the region the EPD hole 9a is formed, because the cell gap is maintained by the patterned spacer 16b in the dummy region, occurrence of the defective cell gap can be prevented.

That is, though dependent on kinds of the protection film, even if an organic insulating material with a thickness in a range of 2μm is used as the protection film and the EPD hole 9a even removes the gate insulating film, resulting in the EPD hole 9a to have a depth close to the cell gap, the occurrence of the defective cell gap caused by the dummy sealant can be prevented, and the gap spot in the active region in the vicinity the EPD hole 9a can be prevented, because the cell gap is maintained by the patterned spacer 16b formed in the dummy region in bonding the two

substrates even if the dummy sealant 20 is formed in the EPD hole 9a.

A method for fabricating the LCD device according to the present invention will be described as follows.

FIG. 9A to FIG. 9D illustrate cross sectional views of the fabrication process for a thin film transistor array substrate according to the present invention. FIG. 10A to FIG. 10C illustrate cross sectional views of the fabrication process for a color filter array substrate according to the present invention.

First, as shown in FIG. 9A, on the first substrate 1 having a dummy region and an active region, a gate line (not shown) and a gate electrode 2a projected from the gate line are formed in the active region, and a gate insulating film 5 is formed on an entire surface of the dummy region and the active region. A semiconductor layer 6 is formed on the gate insulating film over the gate electrode 2a in an island form.

Referring to FIG. 9B, a source electrode 3a projected from the data line 3 is formed at one side of the semiconductor layer 6 in the active region, a drain electrode 3b is formed at an opposite side thereof, and a protection film 7 is formed on an entire surface of the dummy region and the active region.

As shown in FIG. 9C, holes 9 and 9a are formed over the drain electrode 3b and in the dummy region, respectively. The hole over the drain electrode 3b is a contact hole 9 for bringing the drain electrode 3b into contact with the pixel electrode, the hole in the dummy region is the EPD hole 9a for measuring and controlling an extent of etch when the contact hole 9 is formed over the drain electrode 3b. In general, since a pad contact hole is formed by etching the gate insulating film 5 and the protection film 7 in the pad region (not shown), the EPD hole 9a is form by etching the gate insulating film 5 and the protection film 7, too.

Then, a pixel electrode 4 is formed in a pixel region so as to be connected to the drain electrode 3b through the contact hole 9.

Referring to FIG. 9D, an alignment film 8 is formed on an entire surface of the substrate for orienting the liquid crystal, and subjected to rubbing. Then, as shown in FIG. 5, the main sealant 10 and the dummy sealant 20 are formed in the active region and the dummy region, respectively.

Next, a process for fabricating the color filter array will be described.

Referring to FIG. 10A, on the second substrate 11 having the dummy region and the active region, a black matrix layer 12 is formed for shielding a light from parts except the pixel region (pixel electrode) in the active region, and an R/G/B color filter layer 13 is formed for displaying colors in respective pixel regions. Then, a common electrode 14 is formed on an entire surface of the substrate inclusive of the color filter layer 13 for implementing a picture.

Although not shown, for prevention of possible leakage of the light caused by defective orientation in the vicinity of a patterned spacer coming from formation of the patterned spacer and an alignment film, and rubbing the alignment film later, the black matrix layer 12 is formed in a part the patterned spacer is to be formed.

Referring to FIG. 10B, the patterned spacers 16a and 16b are formed on the common electrode 14 with a distance. That is, the patterned spacer 16a or 16b is formed, not only in the active region, but also in the dummy region for prevention of defective cell gap of the dummy sealant caused by the EPD hole 9a.

As shown in FIG. 10C, the alignment film 15 is formed on an entire surface of the substrate inclusive of the patterned spacers 16a and 16b for orienting the liquid crystal, and the alignment film 15 is rubbed.

After dispensing the liquid crystal on the first, or second substrate formed thus, the two substrates are bonded. Of course, the main sealant 10 and the dummy sealant 20 may be formed on the second substrate, and the patterned spacers 16a and 16b may be formed on the first substrate.

Though the embodiments of the present invention have been described only taking the LCD having the liquid crystal dispensing method applied thereto as examples, the patterned spacer may be formed in the dummy region of the LCD having the liquid crystal injecting method applied thereto in which ball spacers are employed, for prevention of occurrence of the defective cell gap of the dummy sealant.

[ADVANTAGES OF THE INVENTION]

The device and method for fabricating a liquid crystal display device of the present invention have the following advantages.

That is, the formation of the patterned spacer in a dummy region permits to prevent occurrence of a defective cell gap by the dummy sealant, because the cell gap is maintained by the patterned spacer formed in the dummy region even if the dummy sealant is formed in the EPD hole in the dummy region.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device comprising:

first and second substrates having a dummy region and an active region;

a main sealant on a periphery of the active region between the first and second substrates;

a dummy sealant in the dummy region between the first and second substrates;

a patterned spacer in the dummy region between the first and second substrates; and

a liquid crystal layer in the active region between the first and second substrates.

2. The device as claimed in claim 1, further comprising an additional patterned spacer in the active region between the first and second substrates.

3. The device as claimed in claim 1, further comprising an EPD hole on the first substrate in the dummy sealant.

4. A method for fabricating a liquid crystal display device, comprising:

providing first and second substrates having a dummy region and an active region;

forming patterned spacers in the dummy region and the active region of one of the first and second substrates;

forming a main sealant on a periphery of the active region and a dummy sealant in the dummy region of one of the first and second substrates;

dispensing liquid crystal on the active region of one of the first and second substrates; and

bonding the first and second substrates.

5. The method as claimed in claim 4, wherein the main sealant and the dummy sealant are formed on the first substrate and the patterned spacers are formed on the second substrate.

6. The method as claimed in claim 4, further comprising, forming a thin film transistor array in the active region of the first substrate, and forming an EPD hole in the dummy region of the first substrate.

7. The method as claimed in claim 6, wherein the dummy sealant is formed at a position corresponding to the EPD hole.

8. A method for fabricating a liquid crystal display device, comprising:

providing first and second substrates having a dummy region and an active region;

forming a thin film transistor array in the active region on the first substrate, the thin film transistor array having a gate line, a data line and source/drain electrodes;

forming a protection film on the first substrate, forming a contact hole to expose the drain electrode, and forming an EPD hole in the dummy region;

forming a pixel electrode in a pixel region so as to be connected to the drain electrode through the contact hole;

forming a color filter array in the active region of the second substrate;

forming a patterned spacer in the dummy region and the active region of the second substrate;

forming a main sealant on a periphery of the active region and a dummy sealant in the dummy region of one of the first and second substrates;

dispensing liquid crystal on one of the first and second substrates; and

bonding the first and second substrates.

9. The method as claimed in claim 8, wherein the dummy sealant is formed at a position corresponding to the EPD hole.

FIG. 1

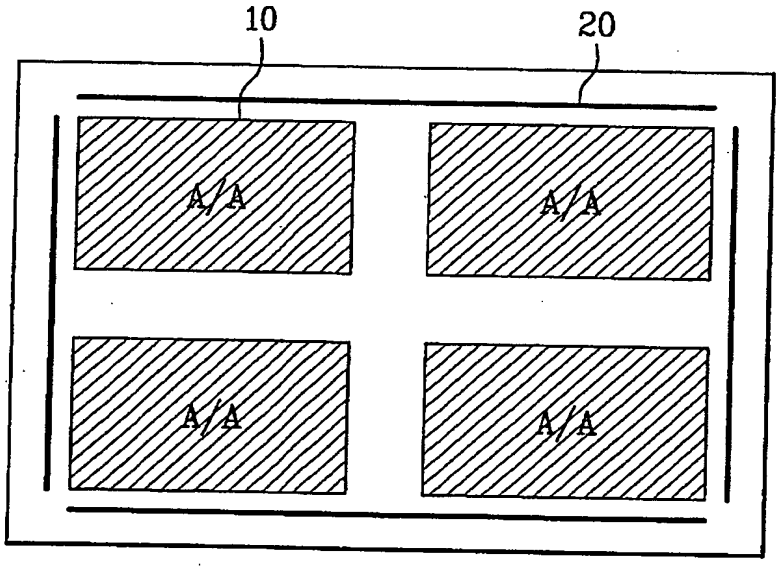

FIG. 2A

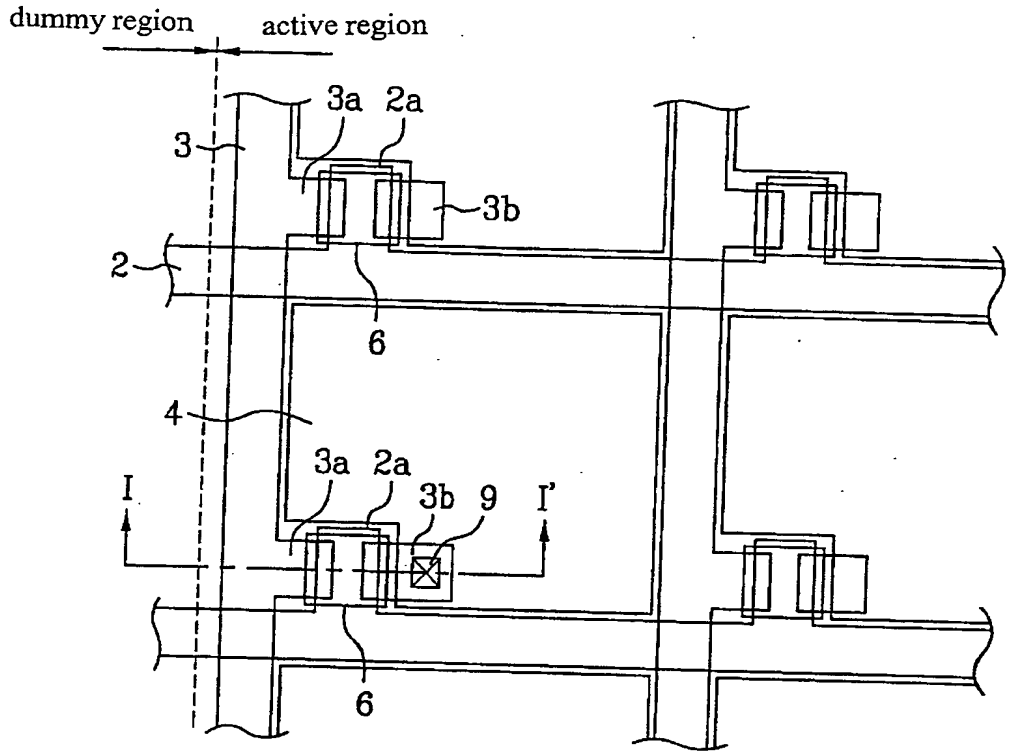
dummy region
active region
3a
2a
3
3b
2
6
4
3a
2a
I
3b
9
I'
6

FIG. 2B

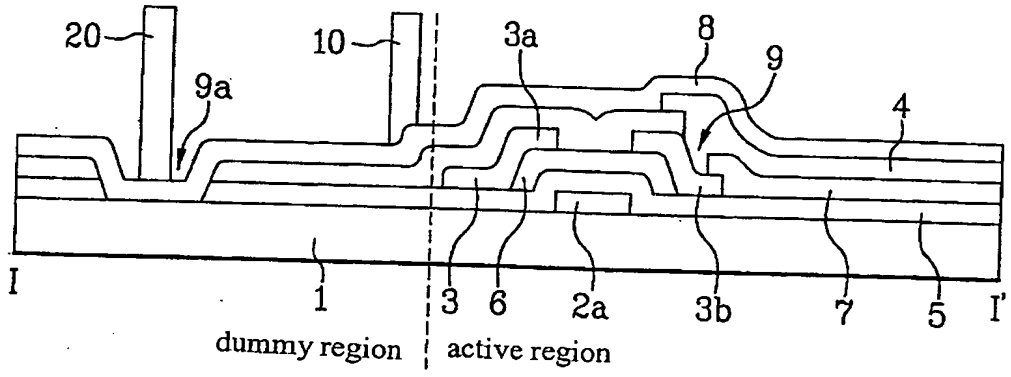
20
10
3a
8
9
9a
4
I
1
3
6
2a
3b
7
5
I'
dummy region
active region

FIG. 3A

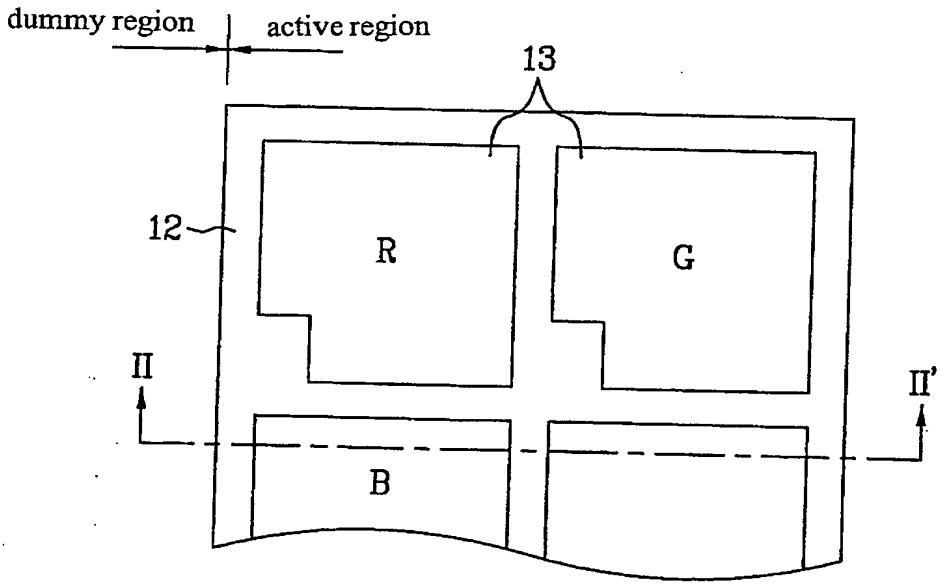
dummy region
active region
13
12
R
G
II
II'
B

FIG. 3B

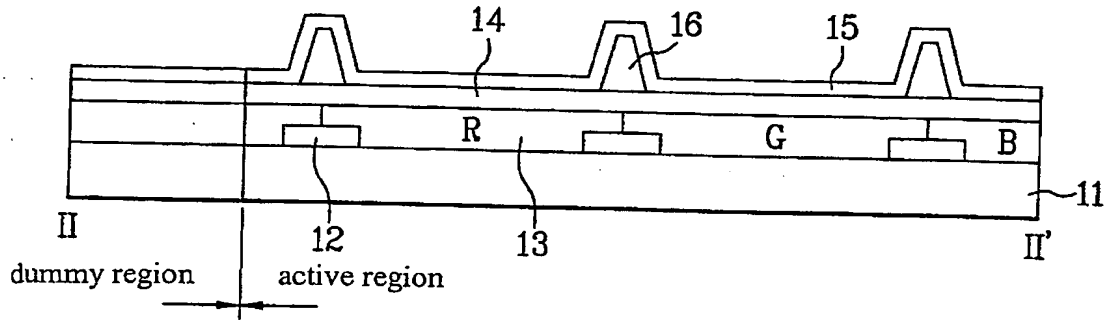
14
16
15
R
G
B
11
II
12
13
II'
dummy region
active region

FIG. 4A

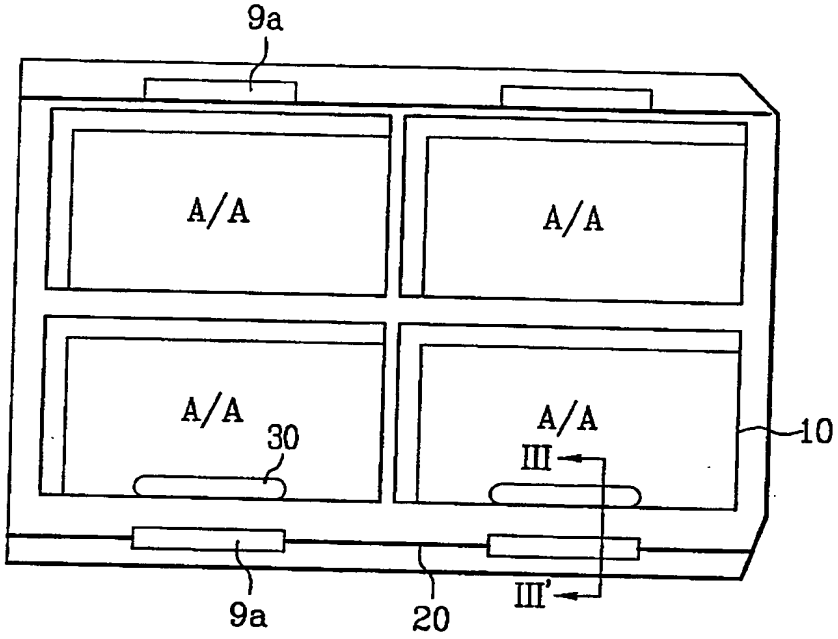

FIG. 4B

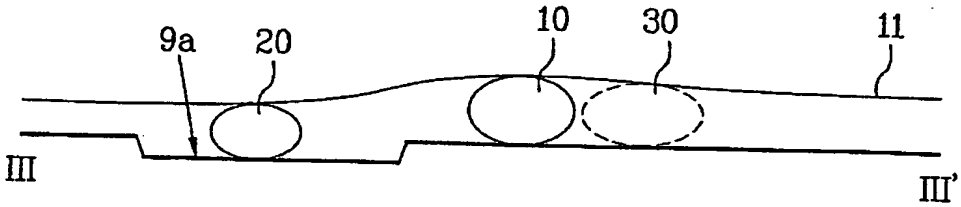

FIG. 5

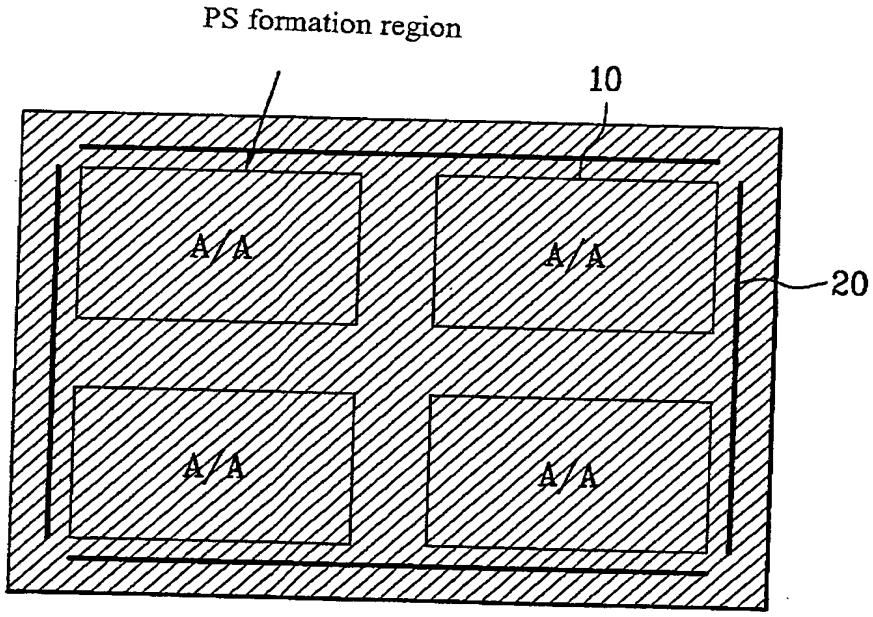

FIG. 6A

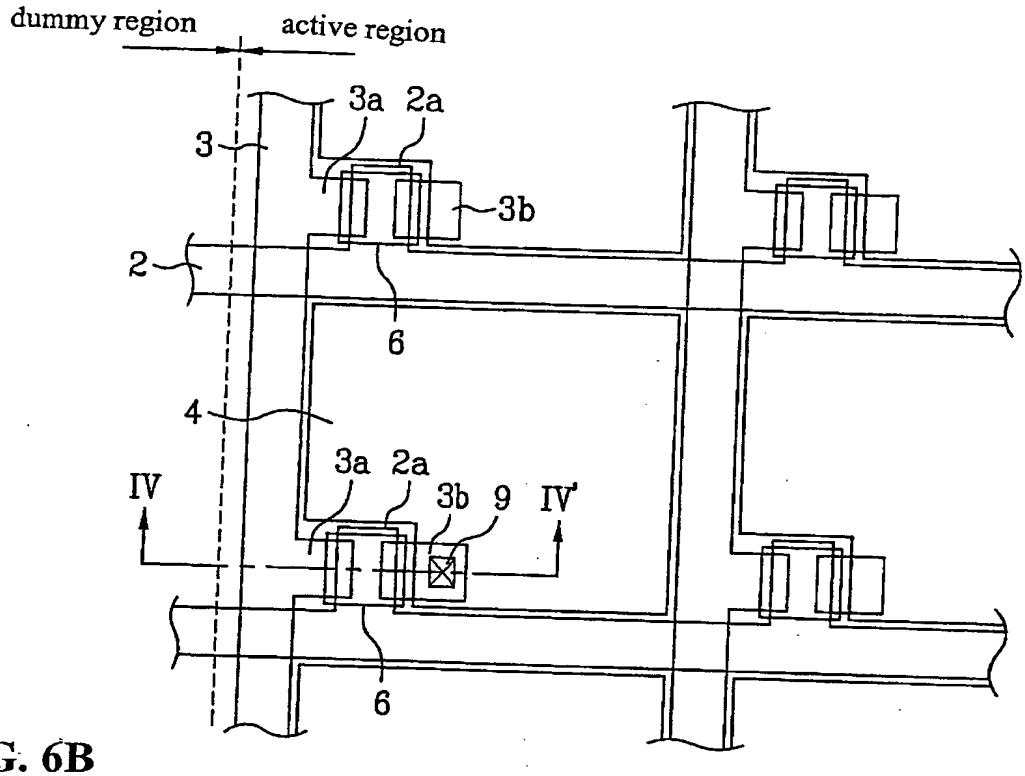
dummy region
active region
3a
2a
3
3b
2
6
4
3a
2a
IV
3b
9
IV'
6

FIG. 6B

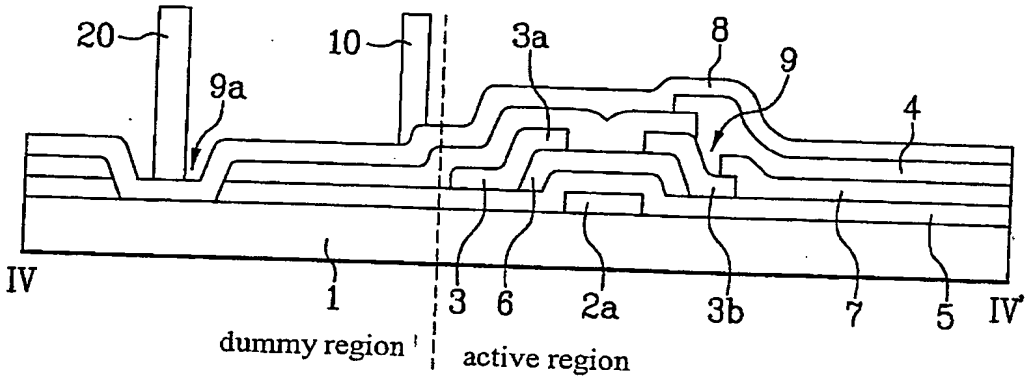
20
10
3a
8
9
9a
4
IV
1
3
6
2a
3b
7
5
IV'
dummy region
active region

FIG. 7A

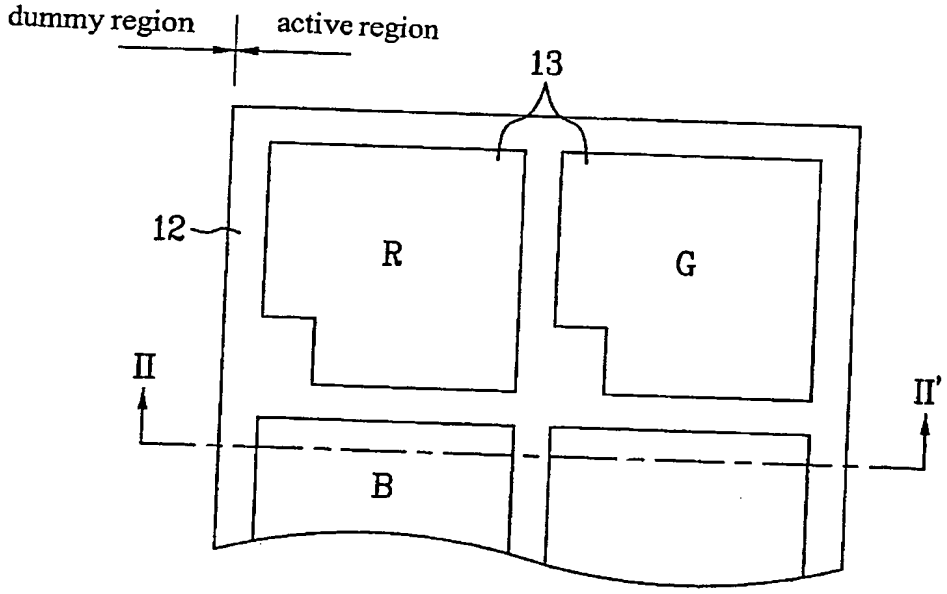
dummy region
active region
13
12
R
G
II
II'
B

FIG. 7B

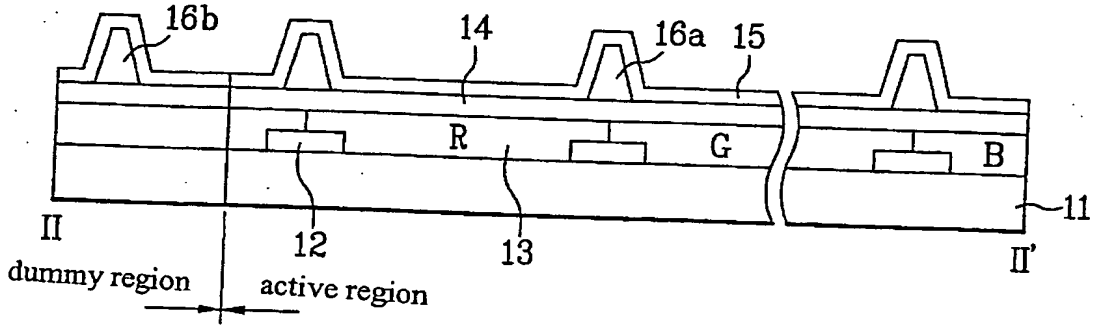
16b
14
16a
15
R
G
B
11
II
12
13
II'
dummy region
active region

FIG. 8

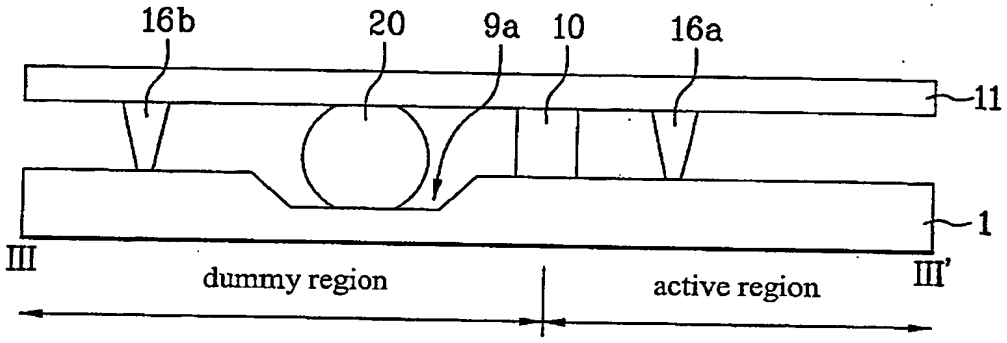

FIG. 9A

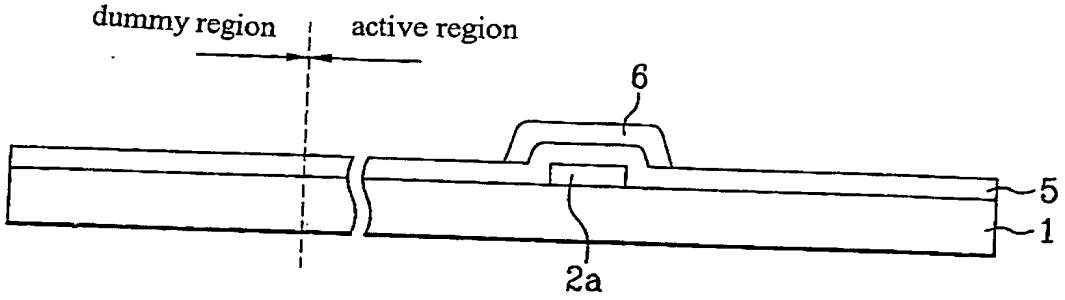

FIG. 9B

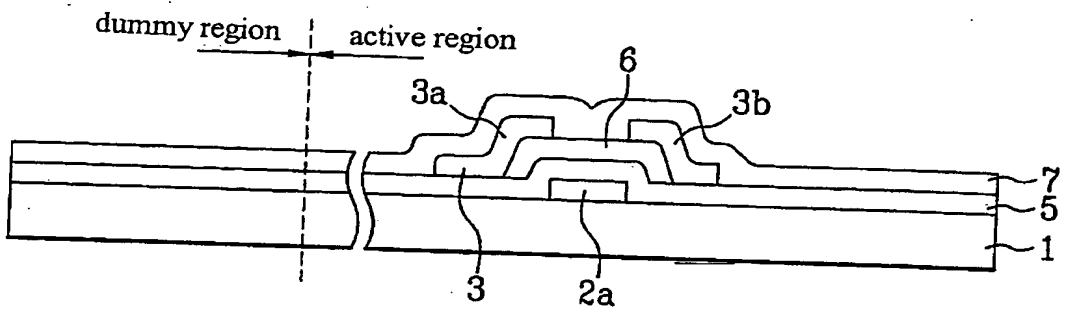

FIG. 9C

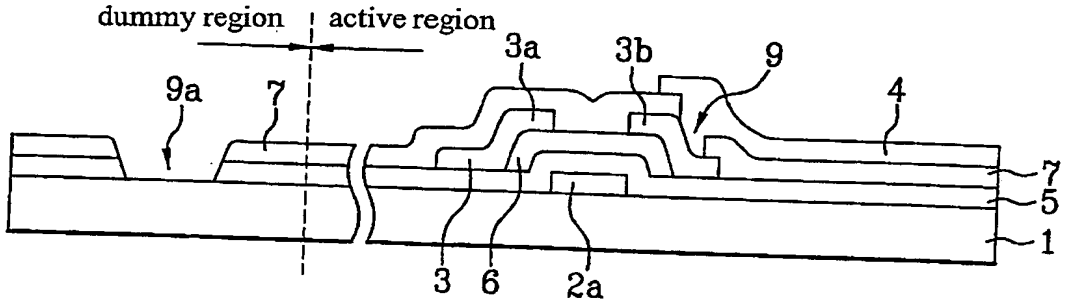

FIG. 9D

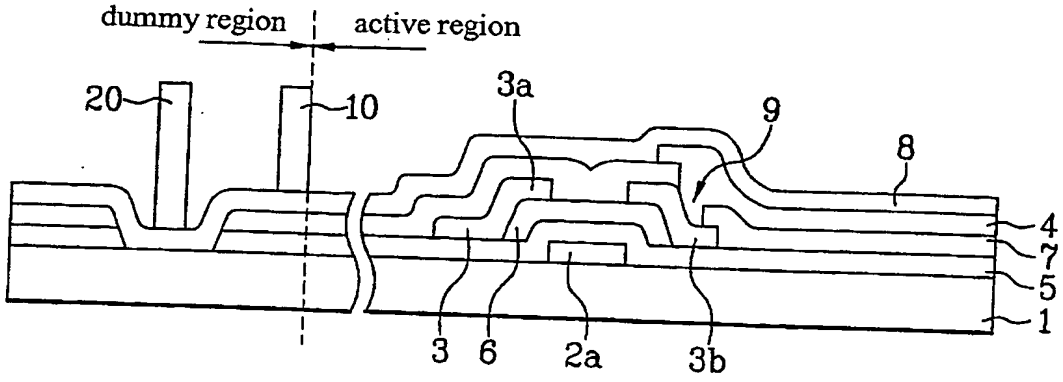

FIG. 10A

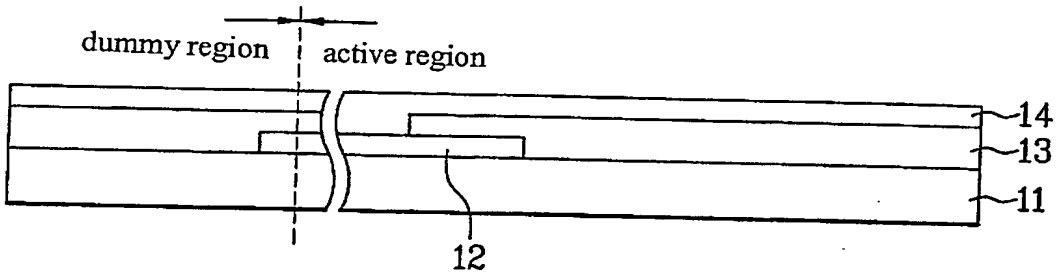

FIG. 10B

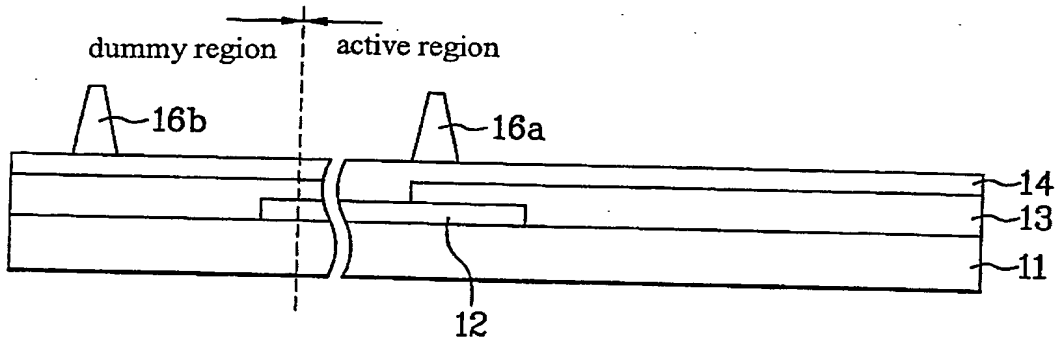

FIG. 10C